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Design and Development of R-load Monitoring and Control Interface for Optimization of Pre-EMC Compliance Test Laboratory

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Abstract— **During electromagnetic interference (EMI) noise immunity tests of Switched-Mode Power Supply (SMPS), Test Engineers (TE) need to be physically present to manually monitor and control the resistive load (r-load) and fan parameters. This practice is prone to human error and, thus, results in accuracy and safety concerns impacting time-to-market and product development costs. To solve this, an EMI-noise immune interface that supports the existing test automation software to remotely monitor and control r-load and fan parameters was designed and developed. The interface has five blocks: the internal supply circuit, the monitoring circuit, the power control circuit, the microcontroller circuit, and the EMI noise protection and filter circuits. For supplies of internal circuitries, a flyback converter is used to provide isolated biases needed to maintain separation between power and communication circuits. For voltage and current monitoring, sense resistors and differential amplifiers are used taking into consideration the component variations' impact on accuracy. For power control, MOSFET driven by a transistor switch is used taking into consideration the components' electrical stresses. For EMI noise mitigation, filters and protective devices are placed on the power lines and shielded I^2C lines where the interface and test computer communicate. Test results showed that the interface has > 95% monitoring precision and accuracy and has 100% control reliability at operating temperatures from -40˚C to 75˚C. Furthermore, it is compliant to class B EMI noise emission and level 3 EMI noise immunity test standards. Therefore, the interface, together with the existing test automation software, may be used for EMI noise immunity tests improving the accuracy of the test while reducing safety risks which optimizes the pre-EMC compliance test laboratory.**

Keywords—Switched-Mode Power Supply, Electromagnetic Compatibility, R-load Monitoring and Control

I. INTRODUCTION

SMPS converts an unregulated AC/DC input voltage to a regulated DC output voltage to power most electronic systems of today. They are widely used in various fields such as in industrial, information technology, and medical industries due to their small size, lightweight, and high efficiency which are the results of their inherent design characteristics, in particular, their internal circuitries high-frequency switching operation. Contrariwise, this high-frequency switching operation is also the cause of their most cited issue – the EMI noise [1].

SMPS either emits EMI noise that interferes with the operation of nearby electronic systems or is exposed to external EMI noise that interferes with its operation. Either way, its impact can be detrimental and, thus, must be minimized if cannot be eliminated. For this reason, SMPS must comply with EMC standards specifically, International Electro-Technical Commission (IEC) and Comité International Special des Perturbations Radio Electriques (CISPR) standards, before putting them on the market [2].

With EMC tests typically taking over at least a week with a cost of up to $2,500 per day, a company needs to invest a total of $12,500 excluding engineering time costs, engineering travel costs, and shipping costs. Being naturally long and expensive, the goal is to pass the first attempt, however, recent studies published by third-party EMC compliance test laboratories show that nearly 50% of products fail EMC compliance tests the first time. This means that another round of design, development, and testing must be done impacting time-to-market and product development cost – risks that could be mitigated by integrating pre-EMC compliance test [3].

Pre-EMC compliance test simulates in-house the final EMC compliance test for early detection and correction of EMC-related concerns. In a case study conducted by Dannan of Diversey Inc., doing pre-EMC compliance tests could give a lead time difference of 6 weeks and cost savings of up to $48,000. This proves that while integrating pre-EMC compliance tests requires additional time and cost investments, it is worth less than what will be incurred if the product fails on the final EMC compliance test. Therefore, the pre-EMC compliance test laboratory must be fully optimized [3].

One challenge in pre-EMC compliance test laboratory optimization is monitoring the parameters of the EUT [4]. For SMPS, this is centered around the r-load used to simulate the power drawn by the EUT's end application. TE must be present for the entire test duration to (1) closely monitor using an oscilloscope the voltage across and current drawn by r-load to determine whether EUT is operating per specification and (2) closely monitor using a power source the voltage across and current drawn by r-load fan to determine whether the latter is cooling down the r-load. Should there be any

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instability, TE needs to promptly turn off the power source of the EUT to prevent further repercussions.

may result in EUT being falsely declared passing. Undetected instability on the r-load fan parameters may result in a fire outbreak. For these reasons, should the TE need to leave for whatever reason, the test needs to be stopped leaving the test set-up idle. This limits the optimization of the pre-EMC compliance test laboratory.

While there are test automation software to take over the job of the TE, they are not supported by existing interfaces such as oscilloscopes and power sources due to the EMI noise paths that the latter introduced. Either this affects the operation of the interfaces themselves, the operation of the test computer that controls them, or the operation of the EUT being tested. In any case, this will give an inconclusive test result [6].

To minimize the impact of EMI noise paths, the primary solution is the use of EMI noise-immune fiber optic cables to connect the interfaces to the test computer and to the EUT parameters being monitored and controlled [7]. This also supports the use of specialized interfaces such as Teseq's Input/Output Box (IOB) 4000 (a stand-alone battery-operated interface that can monitor up to 12 digital, analog, and optical inputs and can control up to 8 digital outputs) [8] and Teseq's NSG6000 (an interface integrated to EMI noise generator that can monitor up to 5 digital and analog inputs and can control up to 14 digital outputs) [9]. While having excellent performance, the use of fiber optic technology requires expensive equipment [10] – investments that later on have to be added to the product costs which will be paid by the end-users. Despite the cost impact, this only eliminates the EMI

Since it relies heavily on TE's attention, any lapse may cause instability to not be detected and, thus, not be corrected [5]. Undetected instability on r-load parameters

noise path introduced by the oscilloscope but not the EMI noise path introduced by the power sources supplying other auxiliaries such as the r-load fans. With costs outweighing the benefits, most pre-EMC compliance test laboratories settle for traditional methodologies.

To solve the aforementioned concerns, the main objective of this research is to design and develop an EMI-noise immune interface that can precisely and accurately monitor r-load and r-load fan parameters and reliably control EUT power delivery to r-load. The r-load, the r-load fan, and the interface will all be powered by the EUT to eliminate the EMI noise paths introduced by oscilloscopes and power sources which then removes the use of expensive fiber optic technology. This interface will support the use of test automation software in mitigating accuracy and safety concerns due to human error guaranteeing the optimization of the pre-EMC compliance test laboratory, not to mention its possible use for other long tests involved in SPMS qualifications such as thermals, reliability, and safety tests.

II. Methodology

The interface is designed for SMPS-rated 48V with a maximum load of 12.5A (600W). It has five blocks: the internal supply circuit, the voltage and current monitoring circuits, the power control circuit, the microcontroller circuit, and the EMI noise protection and filter circuits. The block diagram is shown in Fig. 1.

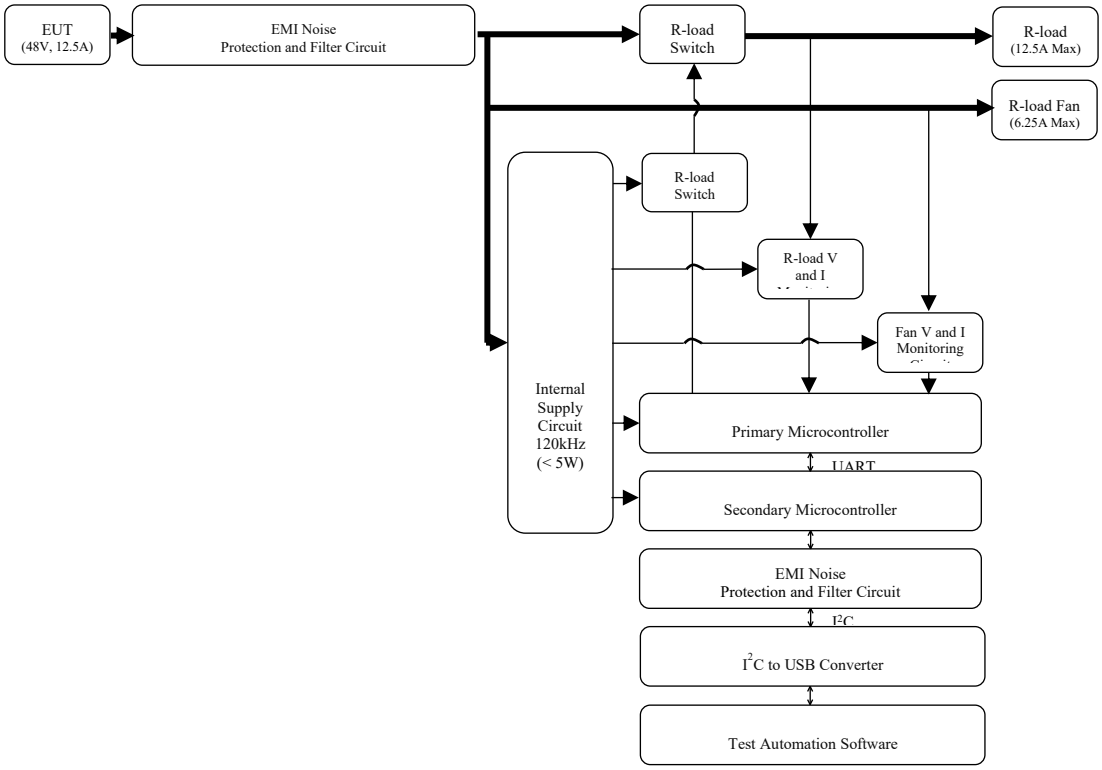


Fig. 1. Interface's Block Diagram

A. The Internal Supply Circuit

The supply circuit powers the internal circuitries. It is a flyback converter operating at 120kHz to provide four galvanically isolated biases – BIAS1 to BIAS4 each rated 12V, 20mA. SIMetrix simulation circuit is shown in Fig. 2.

- The transformer is constructed using AWG#32 wires wound on TP4A-EE16/16/5AZ core with saturation flux density rating of 390mT. With 90µH primary inductance, the computed flux density is 149.47mT which is below the maximum rating.
- The primary switch used is TPK13P25D with $V_{DS(MAX)}$ of 250V and $I_{D(MAX)}$ of 13A. Transient analysis shows that the electrical stresses are below maximum ratings with $V_{DS(MAX\_SIM)}$ of 77.50V and $I_{D(MAX\_SIM)}$ of 0.51A.
- The secondary switches used are DO219AB with $V_{R(MAX)}$ of 200V and $I_{F(MAX)}$ of 30A. Transient analysis shows that the electrical stresses are below maximum ratings with $V_{R(MAX\_SIM)}$ of 37.80V and $I_{F(MAX\_SIM)}$ of 0.22A.
- The controller used is UC2844 having an inner current control loop to determine the response to input voltage changes and an outer voltage control loop to determine the response to load changes. AC analysis shows that with the computed values using the application note's step-by-step design procedure, the control loop is stable with a gain margin of 40.60dB and a phase margin of 58.34˚.

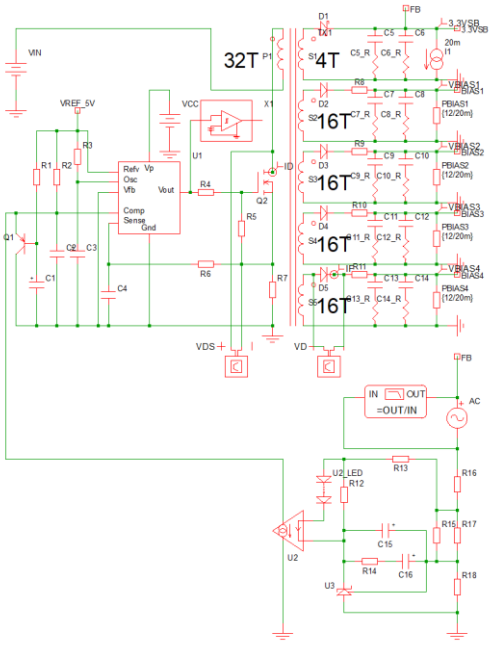


Fig.2. Internal Supply Circuit

Transient analysis shows that the regulation of BIAS1 to BIAS4 is 14.25% (13.71V vs. 12V).

B. The Voltage and Current Monitoring Circuit

The monitoring circuit reports the voltage across and the current drawn by the r-load and its fan. SIMetrix simulation circuits are shown in Fig. 3 and Fig. 4.

- For voltage sensing, resistors are placed across the r-load and fan. The voltage drops across the lower resistors are then fed to AMC1200B – a differential amplifier with a fixed gain of 4 plus 1.3. The outputs of the differential amplifiers are then fed to the primary microcontroller for analog-to-digital conversion. The primary microcontroller sends the data to the secondary microcontroller via UART communication lines. The secondary microcontroller sends the data to the test computer via the I^2C communication lines. The received data is the reported voltage across the r-load and its fan.

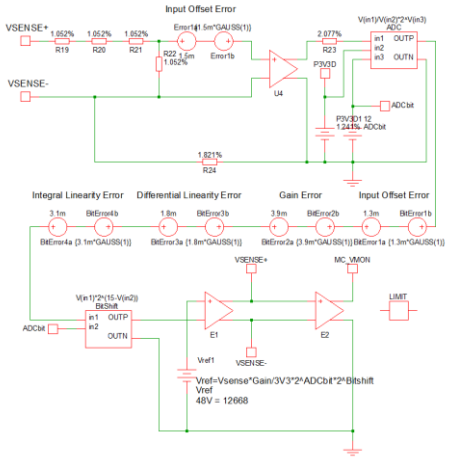


Fig. 3. Voltage Monitoring Circuit

- For current sensing, resistors are placed in series with the r-load and fan. The voltage drops across the resistors are fed to INA214 – a current sense amplifier with a fixed gain of 100. The outputs of the current sense amplifiers are then fed to the microcontroller for analog-to-digital conversion. The primary microcontroller sends the data to the secondary microcontroller via UART communication lines. The secondary microcontroller sends the data to the test computer via the I^2C communication lines. The received data is the reported current drawn by the r-load and its fan.

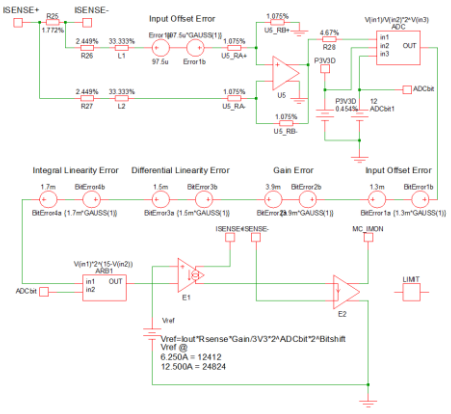


Fig. 4. Current Monitoring Circuit

Monte Carlo analysis shows that the errors introduced on accuracy by the root sum of square tolerance of resistors, error of sense amplifiers, and errors of microcontroller are 1.97% (48.76V or 46.88V vs. 47.82V) for voltage monitoring, 2.08% and 2.23% for current monitoring at 12.5A (12.78A or 12.25A vs. 12.52A) and 6.25A (6.40A or 6.12A vs. 6.26A).

C. The Power Control Circuit

The control circuit delivers power to the r-load at normal conditions and cuts off the power to the r-load at fault conditions. SIMetrix simulation circuit is shown in Fig. 5.

- The output switch drive is a transistor switch. At normal conditions, the microcontroller pulls EN to PGND, pulling VGS to BIAS1, turning on the output switch, and, thus, delivering power to the r-load. At fault conditions, the microcontroller pulls EN to P3V3D pulling VGS to PGND, turning off the output switch and, thus, cutting off the power to the r-load.
- The output switch used is BSC035N10NS5 with $V_{DS(MAX)}$ of 100V and $I_{D(MAX)}$ of 100A. Transient analysis shows that the electrical stresses are below maximum ratings with $V_{DS(MAX\_SIM)}$ of 48.07V and $I_{D(MAX\_SIM)}$ of 12.49A.

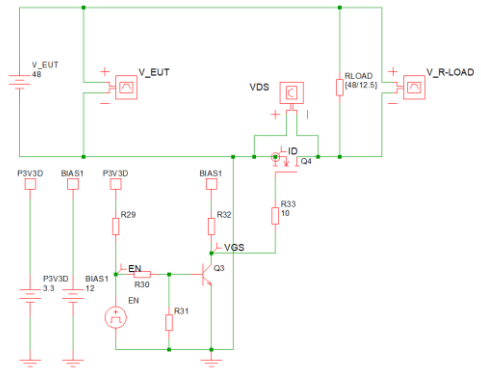


Fig. 5. Power Control Circuit

Transient analysis shows that the reliability of EN signal vs. output switch state response is 100% (drive period is 100ms with a duty cycle of 50%).

D. The Microcontroller Circuit

The microcontroller circuit manages the monitoring and control. The block diagram is shown in Fig. 6.

- The primary microcontroller has two output managers, a primary data manager, and a slave adaptable data protocol (ADP) manager.
- The secondary microcontroller has an I²C manager, a secondary data manager, and a master ADP manager.
- When test automation software sends either a monitoring or a control command via I²C communication lines, the secondary microcontroller communicates with the primary microcontroller via UART to pull or load data, respectively. Optocouplers are used to maintain the galvanic isolation between power and communication circuits.

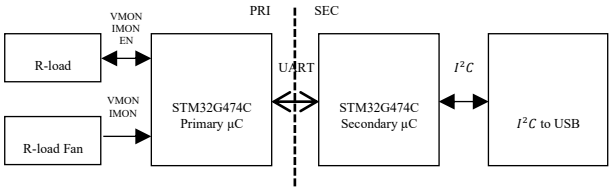


Fig. 6. Microcontroller Circuit Block Diagram

E. The EMI Noise Mitigation Circuit

The filter circuit attenuates the high-frequency EMI noises going in and out of the interface while the protection circuit clamps the high-voltage EMI noises going in and out of the interface.

- On the power lines, LC filters (180µH and 220µF) are placed across L+ and L- to attenuate differential mode noises while C filters (100nF) are placed across L+/L- and GND to attenuate common-mode noises. Metal oxide varistors (TVR14820) connected across L+ to L- and L+/L- to GND are used as first-level protection while two transient voltage suppressors (8.0SMDJ28CA) connected in series across L+ and L- are used as second-level protection. The circuit is shown in Fig. 7.

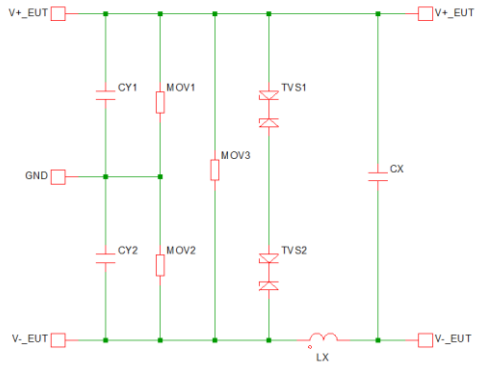


Fig. 7. Power Lines EMI Noise Filter and Protection Circuit

- On the I²C communication lines, ferrite cores HF40BB3.5x5x1.3 are placed on SDA and SCL lines giving an attenuation of > 30dB at frequencies > 30MHz. Electrostatic discharge (ESD) diodes (PESD3V3S5UD) connected across SDA/SCL to SGND are used as first-level protection. RC filters (100Ω and 100pF) also connected across SDA/SCL to SGND are used for additional filtering and as second-level protection. The circuit is shown in Fig. 8.

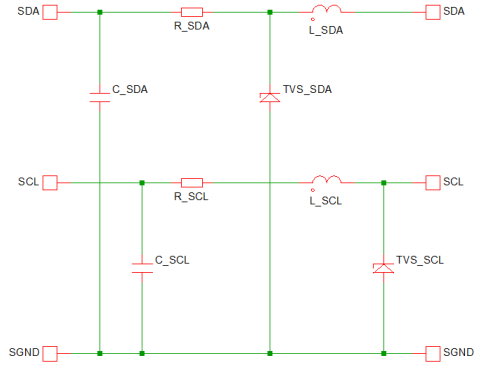


Fig. 8. I²C Lines EMI Noise Filter and Protection Circuit

On PCB layout, best practices to consider EMC are also applied. To prevent end-to-end EMI noise coupling, power lines EMI noise protection devices and filters are placed very near the input side of the PCB with enough separation from other circuits placed on the output side of the PCB. To reduce the impact of high di/dt loops, which in this case are on the primary and secondary switches of the internal supply circuit, high-frequency bypass capacitors are added. To reduce the impact of a high dV/dt node, which in this case is on the primary switch of the internal supply circuit, Resistor-Capacitor-Diode (RCD) snubbers are added.

The interface is placed on a metal enclosure and its I^2C communication lines are shielded to prevent generated EMI noise from radiating or external EMI noise from penetrating. Finally, it is placed on acrylic housing for additional mechanical protection. The actual interface with its connections to r-load, fan, PSU, and test computer is shown in Fig. 9.

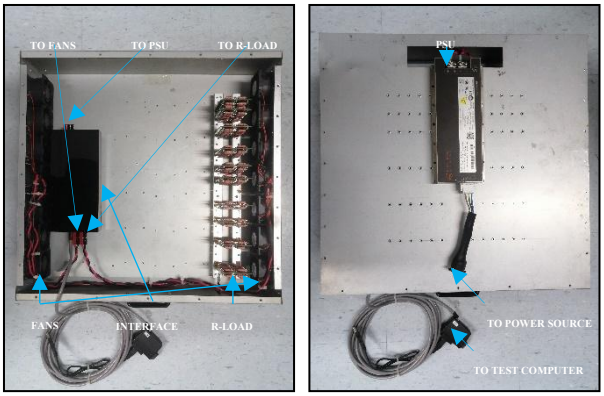


Fig. 9. The Interface

III. Test Results

The proposed interface is tested to validate its performance. Unless otherwise stated, the general test set-up used is shown in Fig. 10. The interface is placed inside a chamber to control the operating temperature. Power source and e-loads are used to vary the input and load of the interface, respectively.

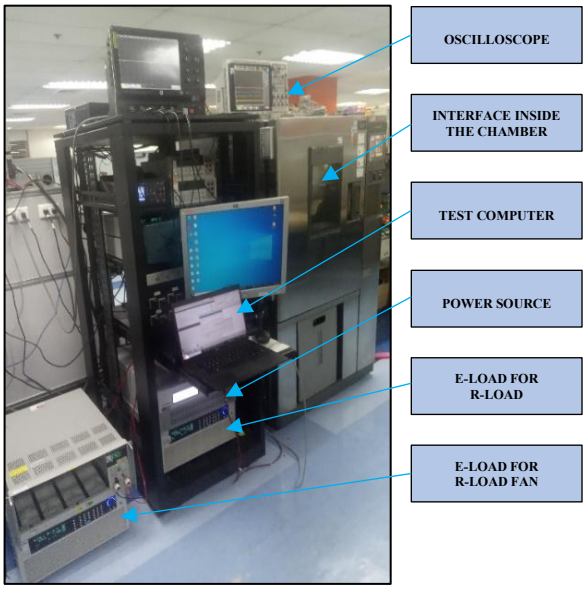


Fig. 10. Test Set-up

A. Internal Supplies Regulation

A 4-channel oscilloscope is used to measure the voltages of the internal supplies.

Fig. 11 shows that the internal supplies regulation at different operating temperatures is less than 20%. At 25˚C, 12.5A load, regulations are 17.17% (14.06V vs. 12V), 9.83% (13.18V vs. 12V), 1.5% (11.82V vs. 12V) and 2.25% (11.73V vs. 12V) for BIAS1 to BIAS4, respectively.

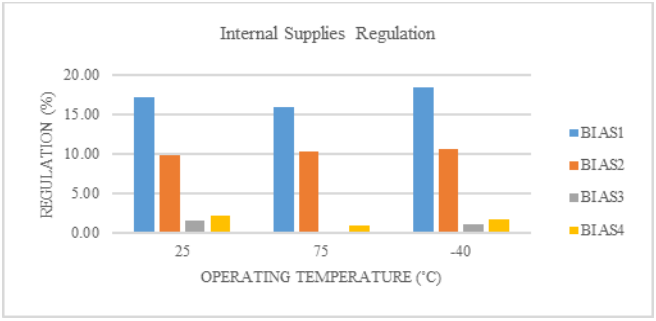
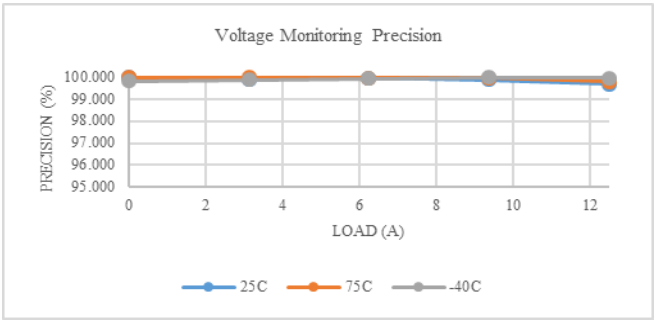


Fig. 11. Internal Supplies Regulation

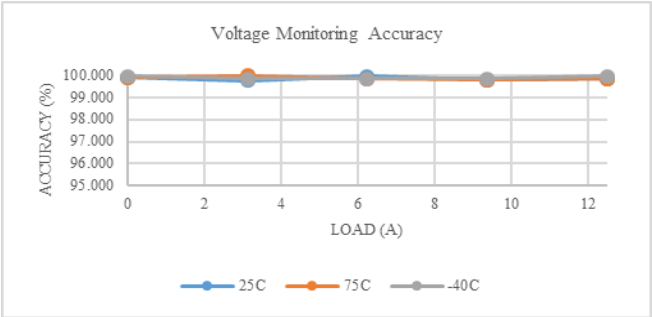
B. Voltage and Current Monitoring Precision and Accuracy

For the measurement of actual voltage and current, e-load voltage sensing (0.015% accuracy) and current sensing (0.04% accuracy) are used. For the measurement of reported voltage and current, test automation software sends a command over the I^2C communication lines. As a response, the interface sends the requested data which are then interpreted then saved.

Fig. 12 shows that the voltage monitoring precision and accuracy at different operating temperatures are > 99%. At 25˚C, 12.5A load, precision and accuracy are 99.674% and 99.834% (47.421V vs. 48V), respectively.



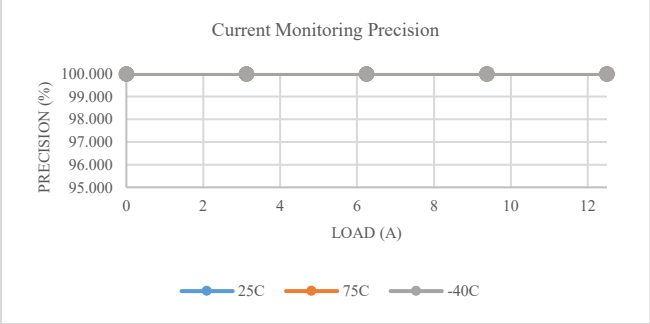
(a)



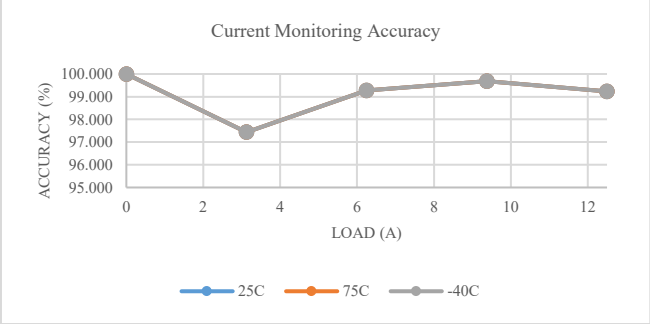
(b)

Fig. 12. Voltage Monitoring (a) Precision and (b) Accuracy

Fig. 13 shows that the current monitoring precision and accuracy at different operating temperatures are ≥ 95%. At 25˚C, 12.5A load, precision, and accuracy are 100% and 99.240% (12.4A vs. 12.5A), respectively.



(a)



(b)

Fig. 13. Current Monitoring (a) Precision and (b) Accuracy

C. *Power Control Reliability*

To simulate fan fault and recovery conditions, e-load is unloaded and loaded, respectively. For the control of the r-load connection to EUT, test automation software sends a command over the I^{2}C communication lines. As a response, the interface asserts or deasserts its EN signal to control the state of the output switches.

Fig. 14 shows that the power control reliability at different operating temperatures is 100%.

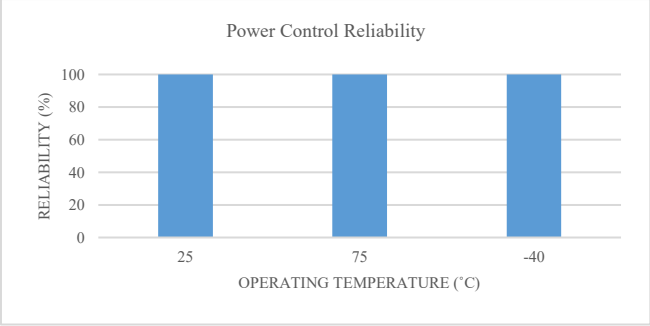


Fig. 14. Power Control Reliability

D. *EMI Noise Emission*

For conducted EMI noise emission, the test set-up is shown in Fig. 15. The interface, connected to the r-load for loading and to the laptop for I^{2}C communications, is placed inside the chamber. It is then interfaced to the LISN which connects it to the power source and the EMI noise receiver both located outside the chamber. ELEKTRA is used to automatically control the EMI noise receiver (Rohde & Schwarz EPL) to measure and analyze EMI noise from 150kHz to 30MHz.

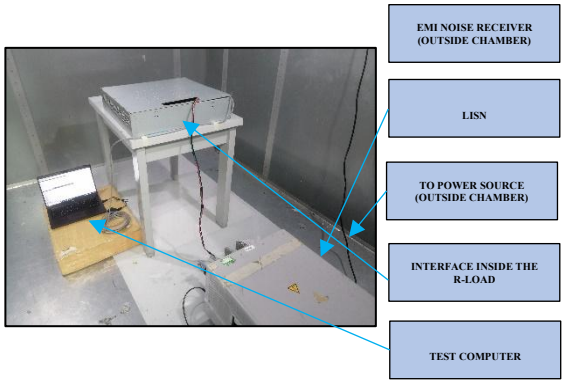
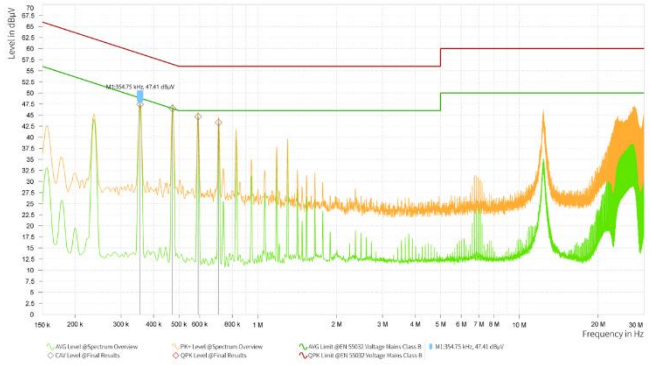


Fig. 15. Conducted EMI Noise Emission Test Set-up

Fig. 16. shows that the interface loading 12.5A is passing the conducted EMI noise emission test per Class B CISPR32 test standard. Worst-case is at 472kHz.

(a)



(b)

Fig. 16. Conducted EMI Noise Emission at (a) L+ and (b) L-

For radiated EMI noise emission, the test set-up is shown in Fig. 17. The interface, connected to the r-load for loading, is placed inside the chamber. Its power cables and I^{2}C communication cables are connected to the power source and laptop, respectively, both located outside the chamber. TOYO is used to automatically control the EMI noise receiver (Rohde & Schwarz EPL) to measure and analyze EMI noise from 30MHz to 1GHz as the antenna (ETS Lindgren 3142E) varies from 1m to 4m height at both horizontal and vertical orientations while the interface is being rotated 360˚.

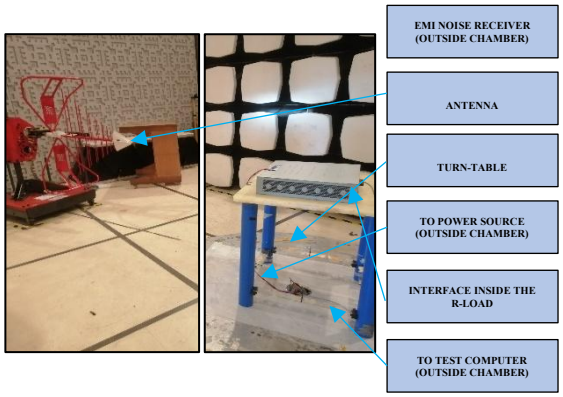


Fig. 17. Radiated EMI Noise Emission Test Set-up

Fig. 18 shows that the interface loading 12.5A is passing the radiated EMI noise emission test per Class B CISPR32 test standard. Worst-case is at 75.348MHz.

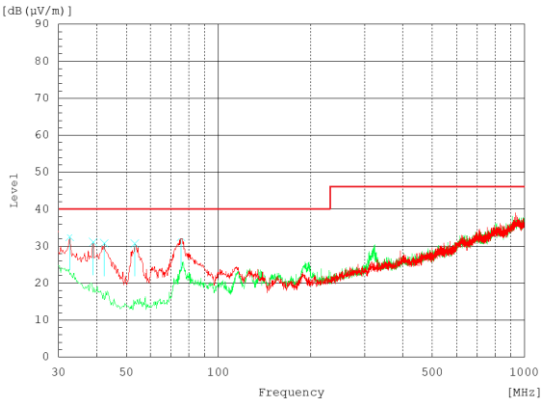


Fig. 18. Radiated EMI Noise Emission at Horizontal (Green) and Vertical (Red) Antenna Orientation

E. EMI Noise Immunity

For all EMI noise immunity tests, the interface is connected to the r-load for loading, to the laptop for I^2C communications, and to the power source and PSU to provide power for stand-alone and application testing, respectively.

For ESD immunity test, the test set-up per IEC61000-4-2 is shown in Fig. 19. Noiseken's ESS-2002 is used to generate noise which is being injected into the interface using the ESD gun. The pointed tip is used to inject contact ESD while the rounded tip is used to inject the air ESD.

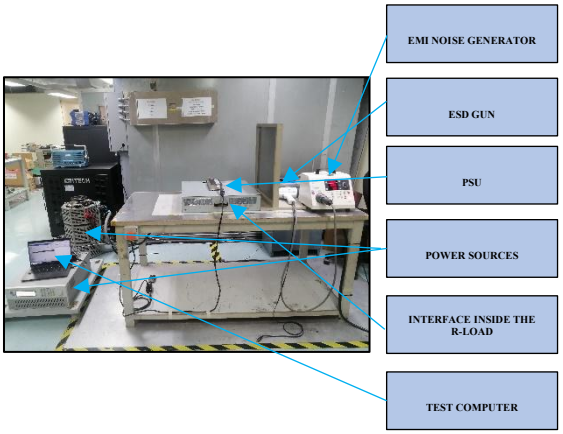


Fig. 19. ESD Immunity Test Set-up

For radiated electrical field immunity test, the test set-up per IEC61000-4-3 is shown in Fig. 20. Teseq's ITS6006 is used to generate noise which is being injected into the interface using a log periodic antenna (Schwarzbeck AM9144) at both horizontal and vertical orientations while the interface is at an angle of 0˚, 90˚, 180˚, and 270˚.

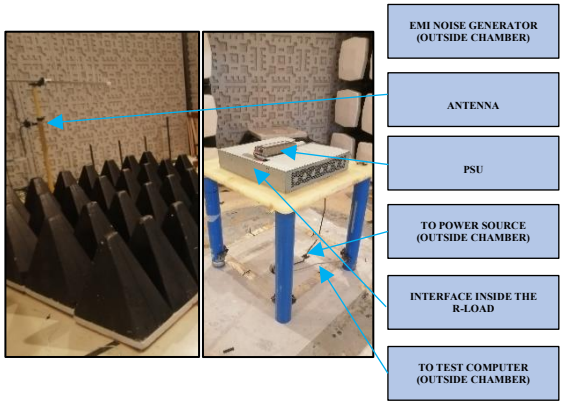


Fig. 20. Radiated Electrical Field Immunity Test Set-up

For electric fast transient (EFT) immunity test, the test set-up per IEC61000-4-4 is shown in Fig. 21. Teseq's NSG3060 is used to generate the noise which is being injected into the interface using CDN 163.

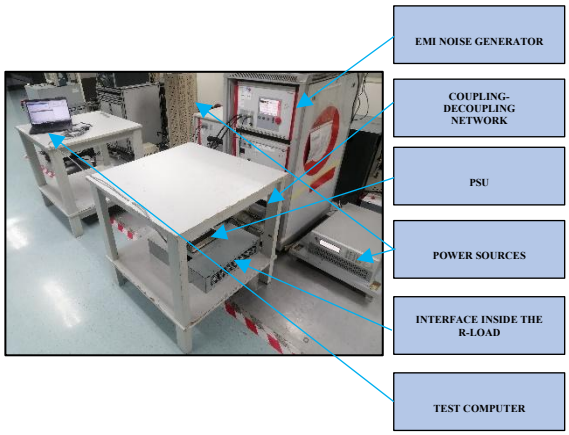


Fig. 21. EFT Immunity Test Set-up

For combinational wave surge immunity test, the test set-up per IEC61000-4-5 is shown in Fig. 22. Teseq's NSG3060 is used to generate the noise which is being injected into the interface using CDN 3063.

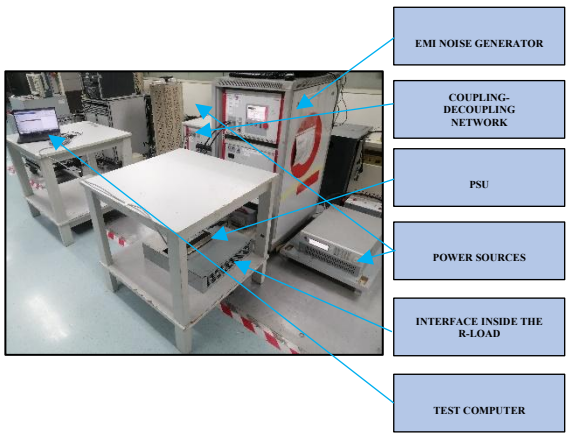


Fig. 22. Combinational Wave Surge Immunity Test Set-up

For conducted RF immunity test, the test set-up per IEC61000-4-6 is shown in Fig. 23. Teseq's NSG4070 is used to generate noise which is injected to the interface using CDN M4-100.

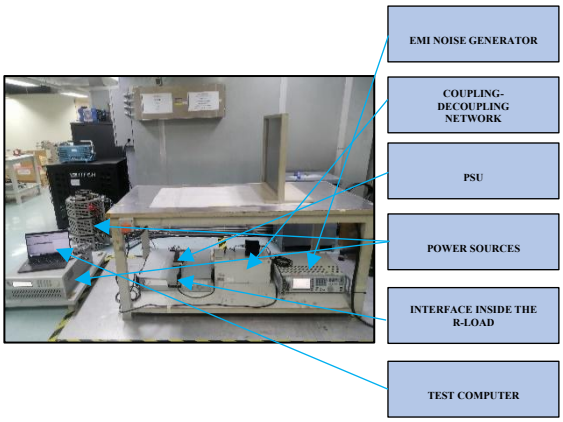


Fig. 23. Conducted RF Immunity Test Set-up

For radiated magnetic field immunity test, the test set-up per IEC61000-4-6 is shown in Fig. 24. Teseq's MFO6501 is used to generate noise which is being injected into the interface using a loop antenna (Teseq INA 702) at X, Y and Z orientations.

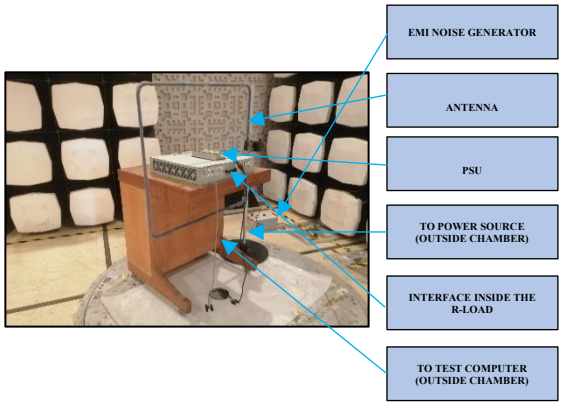


Fig. 24. Radiated Magnetic Field Immunity Test Set-up

The interface's EMI noise immunity test performance criteria are summarized in Table 1

TABLE I. INTERFACE'S EMI NOISE IMMUNITY TEST PERFORMANCE CRITERIA

EMI Noise Immunity Tests (Level 3)	Performance Criteria	
	Stand-Alone	With PSU
Electrostatic Discharge	**A**	**A**
• ±6kV Contact, ±8kV Air	A	A
Radiated Electrical Field	**A**	**A**
• 10V/m (80MHz – 1GHz)	A	A
Electric Fast Transient	**A**	**A**
• ±2kV L+/L-/GND to Ground Plane	A	A
Combinational Wave Surge	**A**	**A**
• ±2kV L+ to L-, L+/L- to GND	A	A
Conducted RF	**A**	**A**
• 10Vrms (150kHz – 80MHz)	A	A
Radiated Magnetic Field	**A**	**A**
• 10A/m (50Hz and 60Hz)	A	A

Note:
Performance Criteria A: Normal performance.
Performance Criteria B: Temporary degradation, self-recoverable.
Performance Criteria C: Temporary loss of function, not self-recoverable.
Performance Criteria D: Permanent damage.

IV. CONCLUSION

An EMI-noise immune interface that can precisely and accurately monitor r-load and fan parameters and reliably control EUT power delivery to r-load is designed and developed. With EUT powering the r-load, the r-load fan, and the interface, EMI noise paths introduced by oscilloscopes and power sources are eliminated which then removes the use of expensive fiber optic technology. With > 95% monitoring precision and accuracy, 100% control reliability, and class B EMI noise emission and level 3 EMI noise immunity test standards compliance, the interface, together with the existing test automation software, can be used to do remote monitoring and control of r-load and fan parameters during EMI noise immunity tests improving the accuracy of the test while reducing safety risks optimizing pre-EMC compliance test laboratory. Consequently, this will benefit the following stakeholders:

- To the TEs, this will allow them to do multitasking which will increase their productivity.
- To the SMPS companies, this will allow them to meet internal and external targets which will strengthen their employees and customers relationships.
- To the end-users, this will allow them to use EMC-compliant PSUs at a reasonable price to meet their respective goals which will collectively benefit the society.

Lastly, this study will support the United Nations Sustainable Development Goal Number 9 by Increasing Resource-use Efficiency (Target 9.4) through Technology Capability Upgrade (Target 9.5).

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